

Amendments to the Claims

1. (Currently amended) A method of creating a record of a debug session for a hardware modeled design on demand, comprising steps:
- selecting a simulation session range;
 - selecting a simulation target range, ~~wherein the simulation target range is~~ within the simulation session range; and
 - generating a value change dump (VCD) file by dumping state information from the hardware modeled design for the selected simulation target range, said generated value change dump (VCD) file being dedicated to the state information in the selected simulation target range and being exclusive of state information outside said selected simulation target range.
2. (Currently amended) The method of claim 1, further comprising steps:
- accessing the VCD file directly from the beginning of the simulation target range to debug the modeled design;
 - recording primary inputs to the hardware modeled design for evaluation;
- and
- recording state information from the hardware modeled design at the beginning of the simulation session range.
3. (Previously presented) The method of claim 21, further comprising steps:
- recording primary inputs to the hardware modeled design for evaluation;
 - recording state information from the hardware modeled design for a portion of the simulation session; and
 - evaluating in the modeled design from simulation time t0 to simulation time t2.
4. (Previously presented) The method of claim 3, wherein the step of generating the VCD file further comprises:
- generating evaluated results from the modeled design based on the recorded primary inputs and recorded state information; and
 - saving the evaluated results of the simulation target range into the VCD file.

5. (Currently amended) The method of claim 1 further comprising ~~comprises~~ steps:
compressing the primary inputs;
recording the compressed primary inputs; and
recording state information from the hardware modeled design at the start of the simulation session range.

6. (Currently amended) The method of claim 5₂ further ~~comprises~~ comprising:
decompressing the compressed primary inputs; and
providing the decompressed primary inputs to the modeled design for evaluation.

7. (Previously presented) The method of claim 1 further comprising:
recording the primary inputs.

8. (Currently amended) The method of claim 21, further comprising steps:
saving state information of the modeled design at simulation time t0 in a first file; and
saving state information of the modeled design at simulation time t3 in a second file.

9. (Currently amended) An electronic design automation system for verifying a user design, comprising:

a computing system including a central processing unit and memory for modeling the user design in software;

an internal bus system coupled to the computing system;

reconfigurable hardware logic coupled to the internal bus system and for modeling at least a portion of the user design in hardware;

control logic coupled to the internal bus system for controlling the delivery of data between the reconfigurable hardware logic and the computing system; and

VCD on-demand logic for recording at least a portion of a selected simulation session range and dumping state information from the hardware model into a VCD file for a selected simulation target range, ~~where~~ wherein the simulation target range is within the simulation session range, and wherein said value change dump (VCD) file is

dedicated to the state information in the selected simulation target range and is exclusive of state information outside said selected simulation target range.

10. (Previously presented) The electronic design automation system of claim 9, wherein the VCD on-demand logic further comprises:

first range selection logic for selecting a simulation session range which begins at a simulation time t_0 and ends at a simulation time t_3 ;

second range selection logic for selecting a simulation target range which begins at a simulation time t_1 and ends at a simulation time t_2 , wherein the simulation time t_1 is greater than or equal to simulation time t_0 and simulation time t_2 is less than or equal to simulation time t_3 ;

dump logic for generating a VCD file of the hardware-modeled design for the selected simulation target range; and

access logic for accessing the VCD file directly from simulation time t_1 to debug the user design.

11. (Previously presented) The electronic design automation system of claim 10, wherein the VCD on-demand logic further comprises:

test bench process for providing primary inputs to the hardware-modeled design for evaluation; and

recording logic in the computing system for recording data associated with at least one parameter in the simulation session range.

12. (Previously presented) The electronic design automation system of claim 11, wherein the VCD on-demand logic further comprises:

process logic in the computing system for loading the recorded data associated with the at least one parameter; and

evaluation logic in the reconfigurable hardware logic for evaluating in the hardware-modeled design the primary inputs from simulation time t_0 to simulation time t_2 .

13. (Previously presented) The electronic design automation system of claim 12, wherein the dump logic dumps the evaluated results from the hardware-modeled design based on the primary inputs during the simulation target range into the VCD file.

14. (Previously presented) The electronic design automation system of claim 13, wherein the recording logic further comprises:
compression logic for compressing the primary inputs;
write logic for writing the compressed primary inputs and state information from the hardware model at simulation time t_0 .

15. (Previously presented) The electronic design automation system of claim 14, wherein the process logic further comprises:
decompression logic for decompressing the compressed primary inputs; and
data transfer logic for delivering the decompressed primary inputs to the hardware-modeled design for evaluation.

C 16. (Previously presented) The electronic design automation system of claim 13, wherein the recording logic further comprises:
write logic for writing the primary inputs and state information from the hardware model at simulation time t_0 .

17. (Previously presented) The electronic design automation system of claim 9, further comprising:
state save logic for saving state information of the hardware-modeled design at simulation time t_0 in a first file and saving state information of the hardware-modeled design at simulation time t_3 in a second file.

18. (Currently amended) A VCD on-demand system for providing evaluated information for a selected simulation target range of simulation times, the evaluation occurring in a hardware model, comprising:
first logic for selecting a simulation session range;
second logic selecting a simulation target range, wherein the simulation target range is within the simulation session range; and
generation logic for generating a VCD file of the evaluated information for the selected simulation target range by dumping state information from the hardware model, wherein said generated value change dump (VCD) file is dedicated to the state information in the selected simulation target range and is exclusive of state information outside said selected simulation target range.

19. (Previously presented) The VCD on-demand system of claim 18, further comprising:

access logic for accessing the VCD file directly from the beginning of the simulation target range to debug the modeled design;

compression logic for receiving and compressing primary input data for the duration of the simulation session range; and

decompression logic for decompressing the compressed primary input data and delivering the decompressed primary input data into the modeled design for evaluation.

20. (Previously presented) The VCD on-demand system of claim 19, wherein the generation logic further comprises:

C dump logic for dumping evaluated information to the VCD file, the evaluated information generated by the evaluation of the decompressed primary inputs by the modeled design.

21. (Previously presented) The method of claim 1, wherein the simulation session range begins at a simulation time t_0 and ends at a simulation time t_3 , and the simulation target range begins at a simulation time t_1 and ends at a simulation time t_2 , wherein the simulation time t_1 is greater than or equal to simulation time t_0 and simulation time t_2 is less than or equal to simulation time t_3 .

22. (Previously presented) The system of claim 18, wherein the simulation session range begins at a simulation time t_0 and ends at a simulation time t_3 , and the simulation target range begins at a simulation time t_1 and ends at a simulation time t_2 , wherein the simulation time t_1 is greater than or equal to simulation time t_0 and simulation time t_2 is less than or equal to simulation time t_3 .